AMENDMENT TO THE DRAWINGS:

As required by the Examiner and subject to the Examiner's approval, Applicant proposes to amend the drawings by labeling Fig. 1 as "Prior Art." An annotated sheet of Fig. 1 showing the change to Fig. 1 in red and a replacement sheet of Fig. 1 incorporating the change to Fig. 1 are enclosed.

ATTACHMENTS:

1. An annotated sheet of Fig. 1 showing the change to Fig. 1 in red; and
2. A replacement sheet of Fig. 1 incorporating the change to Fig. 1.

REMARKS

By this Amendment, Applicant has amended claims 1, 13, and 24 to more appropriately define the invention. Claims 1-31 are pending. Applicant also proposes an amendment to the drawings for the Examiner's approval.

In the Office Action, the Examiner objected to the drawings and required tat Fig. 1 be labeled as Prior Art; rejected claims 1-7, 9, 11-19, 22, and 23 under 35 U.S.C. § 102(b) as anticipated by Gardner et al. (U.S. Patent No. 5,780,340); rejected claims 24-31 under 35 U.S.C. § 102(b) as anticipated by Sugawara et al. (U.S. Patent No. 6,171,916); and rejected claims 8, 10, 20, and 21 under 35 U.S.C. § 103(a) as unpatentable over Gardner et al. in view of *Stanley Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era*, Vol. I, Lattice Press, 1986, pp. 551-555 ("Wolf").

As the Examiner required, Applicant proposes to amend the drawings to label Fig. 1 as "Prior Art" and request that the objection to the drawings be withdrawn.

Applicant respectfully traverses the rejections under 35 U.S.C. § 102(b).

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102, each and every element of the claim in issue must be found, "either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. § 2131, 8th ed., Rev. of May 2004.

The rejection of claims 1-7, 9, 11-19, 22, and 23 under 35 U.S.C. § 102(b) as anticipated by Gardner et al. is improper, because Gardner et al. does not teach each and every element of these claims.

Independent claims 1 and 13 each recite a method for fabricating a semiconductor transistor that includes, inter alia, "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor."

The Examiner considered Gardner et al.'s nitride layer 108 and polysilicon gate electrode 142 as respectively corresponding to Applicant's claimed "second insulating layer" and "conductor." Office Action, page 3. However, even if Gardner et al. teaches "depositing and planarizing" nitride layer 108 and gate electrode 142, this does not form a trench gate comprising nitride layer 108 and gate electrode 142. See Gardner et al., Figs. 1A-1Q. Rather, as Fig. 1O shows, Gardner et al. only teaches a gate composed of gate electrode 142 and gate oxide 136 or a gate composed of gate electrode 144 and gate oxide 138. Therefore, Gardner et al. fails to teach at least "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor," as recited in claims 1 and 13. Claims 1 and 13 are thus allowable over Gardner et al.

Claims 2-7, 9, 11-19, 22, and 23 respectively depend from claims 1 and 13 and are also allowable over Gardner et al. at least because of their dependence from an allowable base claim.

The rejection of claims 24-31 under 35 U.S.C. § 102(b) as anticipated by Sugawara et al. is also improper, because Sugawara et al. does not teach each and every element of these claims.

Claim 24 recites a method for fabricating a semiconductor transistor that includes, inter alia, "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor."

The Examiner alleged that Sugawara et al. teaches "forming a trench gate 22 by depositing and planarizing a second insulating layer 23 and a first conductor 11 on the substrate with the trench (figure 2F; col. , lines 43-49.)" Office Action, page 7. The Examiner apparently considered Sugawara et al.'s side-wall insulating film 23 and polycrystalline silicon film 11 as respectively corresponding to Applicant's claimed "second insulating layer" and "conductor." Applicant disagrees with the Examiner's position.

First, Sugawara et al.'s side-wall insulating film 23 and polycrystalline silicon film 11 do not compose a gate and cannot respectively correspond to Applicant's claimed "second insulating layer" and "conductor." Additionally, even assuming, arguendo, that Sugawara et al. teaches a gate comprising side-wall insulating film 23 and polycrystalline silicon film 11, Sugawara et al. does not teach "planarizing" side-wall insulating film 23. Instead, side-wall insulating film 23 is formed by a thermal treatment of semiconductor substrate 1 "at a temperature of approximately 900° C. in an oxygen atmosphere for several minutes to several tens of minutes." See Sugawara et al., col. 8, ll. 4-11.

Therefore, Sugawara et al. fails to teach at least "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor," as recited in claim 24. Claim 24 is thus allowable over Sugawara et al. Claims 25 and 31 depend from claim 24 and are also allowable over Sugawara et al. at least because of their dependence from an allowable base claim.

Applicant also traverses the rejection of claims 8, 10, 20, and 21 under 35 U.S.C. § 103(a) as unpatentable over Gardner et al. in view of Wolf, because a prima facie case of obviousness has not been established.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. § 2143, 8th ed., Revision of May 2004.

As discussed above, Gardner et al. fails to teach or suggest at least "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor," as recited in claims 1 and 13, from which claims 8, 10, 20, and 21 respectively depend.

Wolf does not cure the deficiencies of Gardner et al. Wolf only discusses dry etching techniques for VLSI fabrication of semiconductor devices. Office Action, page 9. Wolf fails to teach or suggest at least "forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor," as recited in claims 1 and 13.

Therefore, Gardner et al. and Wolf, taken alone or in combination, fail to teach or suggest each and every element of claims 1 and 13. Claims 8, 10, 20, and 21, which depend from claims 1 and 13, are therefore allowable under 35 U.S.C. § 103(a).

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims 1-31.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 11, 2005

By: _____
Qingyu Yin
Ltd. Rec. No.: L0222

ANNOTATED SHEET SHOWING CHANGES

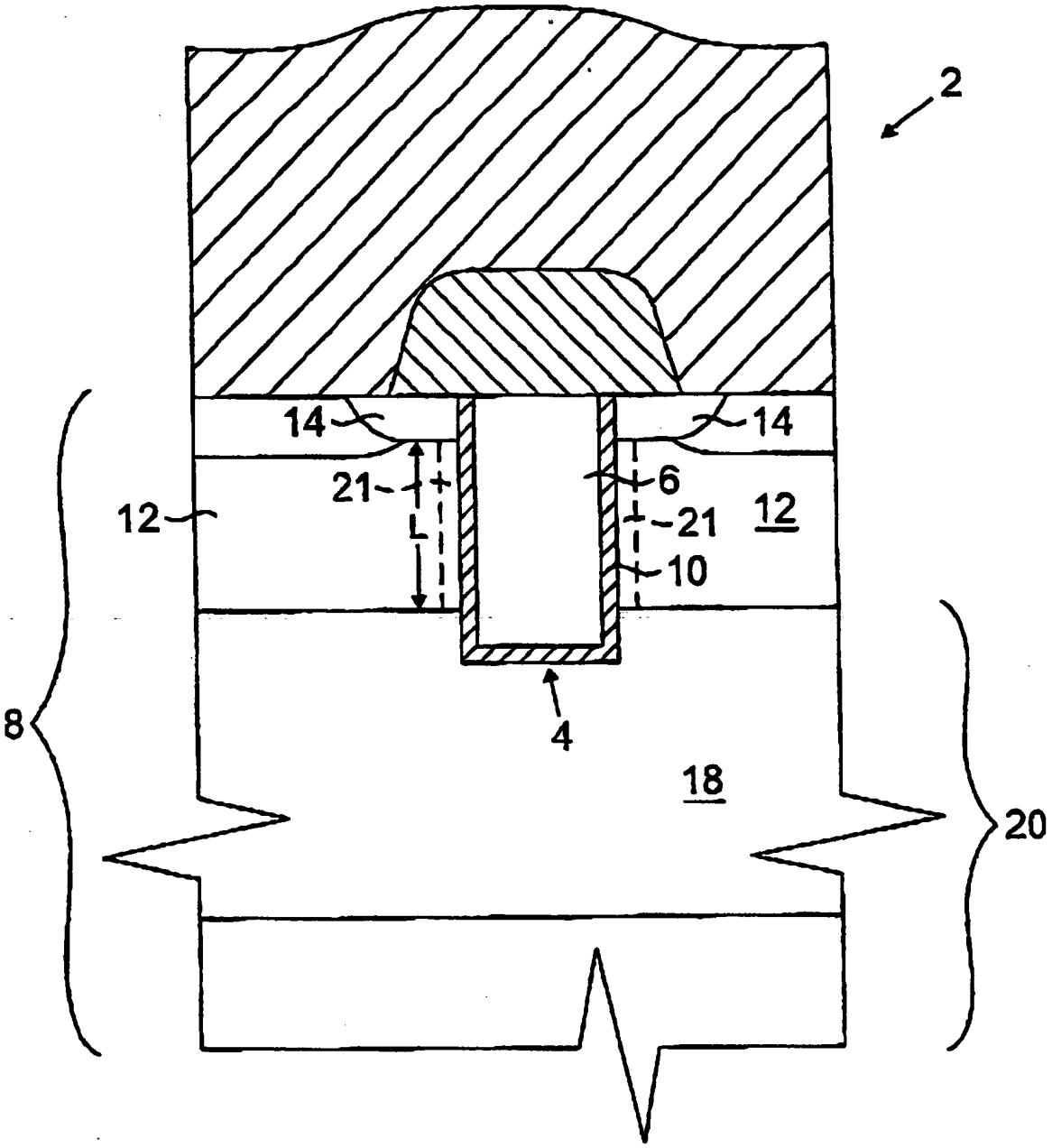

Fig. 1 PRIOR ART